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EXAMINER	
MOYER, MICHAEL J	

ART UNIT	PAPER NUMBER
2675	

DATE MAILED: 10/03/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/876,119	KOMURA ET AL.	
	Examiner	Art Unit	
	Michael J. Moyer	2675	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 October 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,10 and 12-18* is/are rejected.

7)☐ Claim(s) *7-9 and 11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Pre-Amendment

1. The pre-amendment filed on 08 June 2001 has been considered. Before claims 1-18 were pending, now claims 1-18 are still pending. Only claim 14 has been amended because of grammatical errors.

Specification

2. The abstract of the disclosure is objected to because it includes reference numbers. If the application should be allowable the examiner will perform an examiners amendment and delete the reference number. Correction is not required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 5 and 10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The examiner has some questions regarding the following claim. **As pertaining to claim 5,** the value of n should be better defined. Does the value of n of n lines the same value as n times? **As pertaining to claim 10,** the examiner cannot find support for claim 10. I have looked through the figures and the specification to find support for this claim. The examiner requests an explanation or for the applicant to show or point out the support for this claim within the specification.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and

the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Reddy, US 6,175,355 B1 in view of Suzuki, US 5,801,841.

As pertaining to claims 1 and 5, Reddy discloses a display panel with a plurality of pixels arranged in rows and columns. In order to display images, a display framed in formed when each pixel in the display is appropriately modulated according to an image. The displayed image is continually updated by displaying a next display frame in a sequence of display frames. Modulating is accomplished by dividing the display panel into blocks of pixels. Each pixel block preferably includes sixteen pixels arranged in a four-by-four array. The grey scale sequences for pixels in a block are offset from one another by various numbers of sub-frames. This offset is termed pixel dispersion. The amount of pixel dispersion is preferably not related to an order in which the pixels are arranged in rows and columns within the blocks (col. 2, lines 6-19, 50-67; col. 3, lines 1-37; figs 1-3).

As pertaining to claims 1 and 5, Reddy does not disclose allocating the gradation, even though grey scaling can be construed as gradation, of n values which are less then the number of N X N' to each of the pixels of pixel block formed from N X N' pixels.

As pertaining to claims 1 and 5, Suzuki discloses an invention regarding an image signal coding apparatus. In which block truncation coding of an image is divided into pixel blocks (rectangular regions of pixels) and pixels values of a block are approximated by a plurality of representative gradation value and resolution information indicating by which representative value of each pixel is expressed (col. 2, lines 4-8). Figures 13(a) and 13(b) shows an example of coded data and decoded pixel block of the block truncation coding. In the following, it is assumed that the pixel block size is 8 pixels by 8 pixels and each pixel has 8-bit resolution (256 levels). An image is reproduced by replacing positions of pixels having

resolution information 0 with the representative gradation value A of group 1 and positions of pixels having resolution information 1 with the representative gradation value B of group 0 and another example of a configuration of coded data generated by the block truncation coding. The two representative gradation values are assigned 16 bits and the resolution information is assigned 64 bits; that is, one pixel block is coded by use of 80 bits (col. 8, lines 5-25). Also, figures 14-15 represent another example of the second embodiment. Referring to a block diagram of FIG. 14, a configuration of a coding apparatus according to a second embodiment of the invention will I)e described. The components in FIG. 14 that are the same as or similar to those in FIG. 2 are given the same reference numerals and descriptions therefor will be omitted. In FIG. 14, a sub-block dividing section 34 divides a pixel block of m X n pixels (m, n: positive integers) that has been extracted from an image signal by the block extracting section 10 into sub-blocks of p X q pixels (p, q: positive integers smaller than m and n, respectively). The operation of the coding apparatus of the second embodiment will be described with reference to FIGS. 15(a) and 15(b). FIG. 15(a) shows an example in which a block of 8 X 8 pixels is divided into sub-blocks of 4 X 4 pixels. The block truncation coding section 30 performs, for instance, binary block truncation coding on each sub-block. FIG. 15(b) shows an example of coded data produced by binary block truncation coding that is performed on a sub-block basis. For each sub-block, coded data consists of two representative gradation values (2 X 8 bits) and resolution information (4 X 4=16 bits) for 16 pixels. Therefore, the code amount per pixel block is 4 X (16+16)=128 bits (col. 9, lines 28-59). So Suzuki disclose to what is said above that allocating the gradation of n values which are less then the number of N X N' to each of the pixels of pixel block formed from N X N' pixels.

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to combine the gradation technique of Suzuki with the grey scale technique and display of Reddy.

The suggestion/motivation for doing so would have been to provide for a better display that allows for higher resolution, higher definition by using a more reliable grey scale and/or gradation technique.

As pertaining to claim 2, Reddy discloses a display that can be divided in pixel blocks (col. 2, lines 6-19, 50-67; col. 3, lines 1-37; figs 1-3) and Suzuki discloses a gradation technique that can be applied to each divide pixel block (col. 2, lines 4-8; col. 8, lines 5-25; col. 9, lines 28-59; figs. 13-15). Claim 2 is dependent on claim 1 and is rejected on the same basis and what is stated above.

As pertaining to claim 3, Reddy discloses a display that can be divided in pixel blocks that can be of any size (col. 2, lines 50-59), therefore a block can comprise of pixels only being in the same column. Claim 3 is dependent on claim 1 and is rejected on the same basis and what is stated above.

As pertaining to claim 4, Reddy discloses wherein one grey scale of one pixel block is given to all pixels of the block in the next row and columns for the same period or frame as that when the signal is given to the pixel where the one grey scale (col. 2, lines 6-19, 50-67; col. 3, lines 1-37; fig. 1-3) corresponds to pixel block. Suzuki discloses the gradation technique (col. 2, lines 4-8; col. 8, lines 5-25; col. 9, lines 28-59) that can be combined with the grey scale technique of Reddy. Claim 4 is dependent on claim 1 and is rejected on the same basis and what is stated above.

5. **Claims 6, 13, and 15-17** are rejected under 35 U.S.C. 103(a) as being unpatentable over Reddy in view of Suzuki and further in view of Akiyama et al (hereinafter "Akiyama"), US 5,977,940.

As pertaining to claim 6, Reddy discloses a display panel with a plurality of pixels or pixel electrodes arranged in rows and columns in the form of a matrix. In order to display images, a display framed in formed when each pixel in the display is appropriately modulated according to an image. The displayed image is continually updated by displaying a next display frame in a sequence of display frames. Modulating is accomplished by dividing the display panel into blocks of pixels. Each pixel block preferably includes sixteen pixels arranged in a four-by-four array. The grey scale sequences for pixels in a block are offset from one another by various numbers of sub-frames. This offset is termed pixel dispersion. The amount of pixel dispersion is preferably not related to an order in which the pixels are arranged in rows and columns within the blocks (col. 2, lines 6-19, 50-67; col. 3, lines 1-37; figs 1-3).

As pertaining to claim 6, it would be obvious that Reddy display would have the following but he does not disclose an X driver for supplying and X signal; an Y driver for supplying and Y signal; a liquid crystal drive voltage supplying circuit for supplying an LC drive voltage to LC drive line arranged in a column direction; an XY calculating circuit for calculating the X and Y signals; a signal comparator for comparing the output of the XY calculating circuit with a reference voltage and outputting a first voltage when the output of the XY calculating circuit is higher than the reference voltage and a second voltage when the lower than that; a switch for controlling the connection of the pixel electrode to the LC voltage line based on the output of the signal comparator; n-gradation approximation calculating circuit and converting the gradation level of each pixel of each block into n-gradation approximation picture signal

approximated to n values less than N X N' and a signal control circuit for controlling all of the above.

As pertaining to claim 6, Suzuki discloses an n-gradation calculating circuit and converting the gradation level of each pixel of each block into n-gradation approximation picture signal approximated to n values less than N X N' (col. 2, lines 4-8; col. 8, lines 5-25; col. 9, lines 28-59; fig. 2 and 14).

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to combine the n-gradation circuit of Suzuki with the grey scale circuit of Reddy.

The suggestion/motivation for doing so would have been to provide for a better display that allows for higher resolution, higher definition by using a more reliable grey scale and/or gradation technique.

As pertaining to claim 6, Akiyama discloses as figure 9 depicts X driver or gate driver 903 for producing a gate signal or X signal; an Y driver or signal driver or producing a Y signal; timing generating circuit 906 for controlling all of the above. As figure 1A depicts a two transistors 8 and 12 and a storage capacitor 2, which can be construed as XY calculating circuit because they take the X and Y signals, calculates another signal representing them and outputs it to a comparator circuit 15 in which a reference voltage is used to compare it to the calculated output signal from the calculating circuit (col. 9, line 25-col. 10, line 65). Figure 8 depicts an LC driving circuit 204 and Figure 11C-11D depicts switches 52. It would be obvious that Akiyama has many different embodiments in which a different design could be implemented that included all the components in one display.

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to combine the LCD of Akiyama with that of Reddy and Suzuki.

The suggestion/motivation for doing so would have been to provide a display that included all of the components in one display, even though it would be obvious that all TFT-LCD would have all of the components above even though it might not be shown. But by combining Akiyama with Reddy and Suzuki the display is able to produce higher resolution and higher definition displays.

As pertaining to claim 13, Reddy discloses a plurality of row lines and column lines, in which a pixel electrode is provided at the intersection of the row and column lines (col. 2, lines 6-19, 50-67; col. 3, lines 1-37; figs 1-3). Akiyama discloses the same thing but also provides the Y signal, the X signal, pixel electrodes and switching elements at the intersection parts of the rows and columns for controlling the connection of a data signal line and pixel electrode according to the calculating value of corresponding signals (col. 9, line 25-col. 10, line 65; fig. 1A). Claim 13 is dependent on claim 6 and is rejected on the same basis and what is stated above.

As pertaining to claims 15-17, Reddy discloses the image is displayed based upon an image therefore it must be obvious that Reddy would have a picture generating unit and a display controller (col. 2, lines 6-19, 50-67; col. 3, lines 1-37; figs 1-3). Furthermore, Reddy discloses using a grey scale technique for allocating n values to each pixel of a pixel block. Suzuki uses a gradation technique (col. 9, line 25-col. 10, line 65; fig. 1A) that can be combined with Reddy. Whether the display apparatus or picture generating unit or the display controller has the means for allocating gradation it is all the same thing because it is adapted for a displaying a picture using sometime of apparatus. Claims 15-17 are dependent on claim 6 and are rejected on the same basis and what is stated above.

6. **Claims 12, 14 and 18** are rejected under 35 U.S.C. 103(a) as being unpatentable over Reddy as applied to claim 6, in view of Suzuki in view of Akiyama and further in view of Robinder, US 5,485,293.

As pertaining to claim 12, Reddy discloses a display panel with a plurality of pixels or pixel electrodes arranged in rows and columns in the form of a matrix. In order to display images, a display framed in formed when each pixel in the display is appropriately modulated according to an image. The displayed image is continually updated by displaying a next display frame in a sequence of display frames. Modulating is accomplished by dividing the display panel into blocks of pixels. Each pixel block preferably includes sixteen pixels arranged in a four-by-four array. The grey scale sequences for pixels in a block are offset from one another by various numbers of sub-frames. This offset is termed pixel dispersion. The amount of pixel dispersion is preferably not related to an order in which the pixels are arranged in rows and columns within the blocks (col. 2, lines 6-19, 50-67; col. 3, lines 1-37; figs 1-3).

As pertaining to claim 12, it would be obvious that Reddy display would have the following but he does not expressly disclose red, green and blue color pixel electrodes; an X driver for supplying and X signal; an Y driver for supplying and Y signal; a liquid crystal drive voltage supplying circuit for supplying an LC drive voltage to LC drive line arranged in a column direction; an XY calculating circuit for calculating the X and Y signals; a signal comparator for comparing the output of the XY calculating circuit with a reference voltage and outputting a first voltage when the output of the XY calculating circuit is higher than the reference voltage and a second voltage when the lower than that; switches for controlling the connection of the colored pixel electrodes to the LC voltage line based on the output of the signal comparator; n-gradation approximation calculating circuit and converting the gradation level of each pixel of each block

into n-gradation approximation picture signal approximated to n values less than N X N' and a signal control circuit for controlling all of the above.

As pertaining to claim 12, Suzuki discloses an n-gradation calculating circuit and converting the gradation level of each pixel of each block into n-gradation approximation picture signal approximated to n values less than N X N' (col. 2, lines 4-8; col. 8, lines 5-25; col. 9, lines 28-59; fig. 2 and 14).

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to combine the n-gradation circuit of Suzuki with the grey scale circuit of Reddy.

The suggestion/motivation for doing so would have been to provide for a better display that allows for higher resolution, higher definition by using a more reliable grey scale and/or gradation technique.

As pertaining to claim 12, Akiyama discloses as figure 9 depicts X driver or gate driver 903 for producing a gate signal or X signal; an Y driver or signal driver or producing a Y signal; timing generating circuit 906 for controlling all of the above. As figure 1A depicts a two transistors 8 and 12 and a storage capacitor 2, which can be construed as XY calculating circuit because they take the X and Y signals, calculates another signal representing them and outputs it to a comparator circuit 15 in which a reference voltage is used to compare it to the calculated output signal from the calculating circuit (col. 9, line 25-col. 10, line 65). Figure 8 depicts an LC driving circuit 204 and Figure 11C-11D depicts switches 52. It would be obvious that Akiyama has many different embodiments in which a different design could be implemented that included all the components in one display.

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to combine the LCD of Akiyama with that of Reddy and Suzuki.

The suggestion/motivation for doing so would have been to provide a display that included all of the components in one display, even though it would be obvious that all TFT-LCD would have all of the components above even though it might not be shown. But by combining Akiyama with Reddy and Suzuki the display is able to produce higher resolution and higher definition displays.

As pertaining to claim 12, Robinder disclose a liquid crystal display that includes red, green and blue color pixel electrodes and switches with each to the LC drive lines (col. 6, line 19-col. 8, line 1-26; fig. 3).

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to combine the color electrodes and switches of Robinder with the LCD of Reddy, Suzuki and Akiyama.

The suggestion/motivation for doing so would have been to provide a display that able to operate as a color display or monochromatic that also can provide higher resolution and higher definition.

As pertaining to claim 14, Reddy discloses a plurality of row lines and column lines, in which a pixel electrode is provided at the intersection of the row and column lines (col. 2, lines 6-19, 50-67; col. 3, lines 1-37; figs 1-3). Akiyama discloses the same thing but also provides the Y signal, the X signal, pixel electrodes and switching elements at the intersection parts of the rows and columns for controlling the connection of a data signal line and pixel electrode according to the calculating value of corresponding signals (col. 9, line 25-col. 10, line 65; fig. 1A). Furthermore, Robinder discloses red, green and blue color pixel electrodes and corresponding switches (col. 6, line 19-col. 8, line 1-26; fig. 3). Claim 14 is dependent on claim 6 and is rejected on the basis and what is stated above.

As pertaining to claim 18, Reddy discloses a plurality of row lines and column lines, in which a pixel electrode is provided at the intersection of the row and column lines (col. 2, lines 6-19, 50-67; col. 3, lines 1-37; figs 1-3). Akiyama discloses the same thing but also provides the Y signal, the X signal, pixel electrodes and switching elements at the intersection parts of the rows and columns for controlling the connection of a data signal line and pixel electrode according to the calculating value of corresponding signals (col. 9, line 25-col. 10, line 65; fig. 1A). Furthermore, Robinder discloses red, green and blue color pixel electrodes and corresponding switches (col. 6, line 19-col. 8, line 1-26; fig. 3). It would be obvious since Reddy discloses the use of frames and sub-frames that the frame frequency would fall into the range of the limitation.

Allowable Subject Matter

7. **Claims 7-9 and 11** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Wilson, US 6,507,350 B1. Wilson teaches flat panel display drive using sub-sampled YCBCR color signals.

b) Imaizumi et al., US 5,838,455. Imaizumi teaches an image processor with image data compressor capability.

c) Ito et al., US 5,896,137. Ito teaches an image processing apparatus having storage area for efficiently storing two-value and multi-value image data.

d) Hathaway et al., US 6,560,375 B1. Hathaway teaches video image stabilization and registration.

e) Suzuki et al., US 5,754,698. Suzuki teaches image signal encoding device having first and second encoding means.

f) Honma et al., US 5,903,360. Honma teaches discriminating an image data characteristic and controlling storage of the data accordingly.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Michael J. Moyer** whose telephone number is **(703) 305-2099.** The examiner can normally be reached Monday-Friday, 8:30am-5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Steven Saras**, can be reached at **(703) 305-9720.**

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to: (703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the **Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.**

Michael J. Moyer
Examiner
Art Unit 2675

MJM
September 25, 2003

STEVEN SARAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600